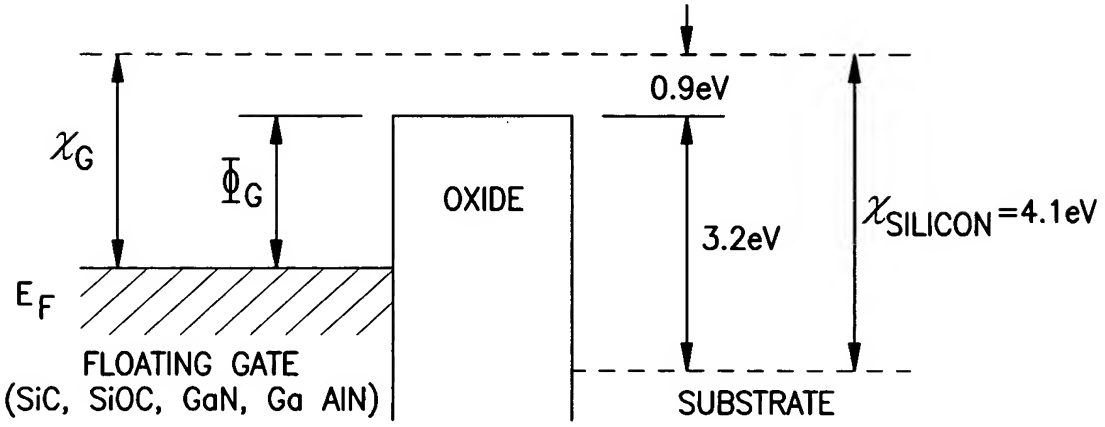

FIG. 1A
(PRIOR ART)

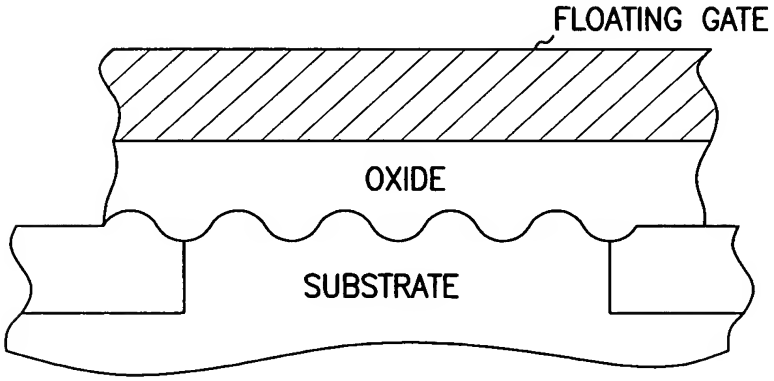

FIG. 1B
(PRIOR ART)

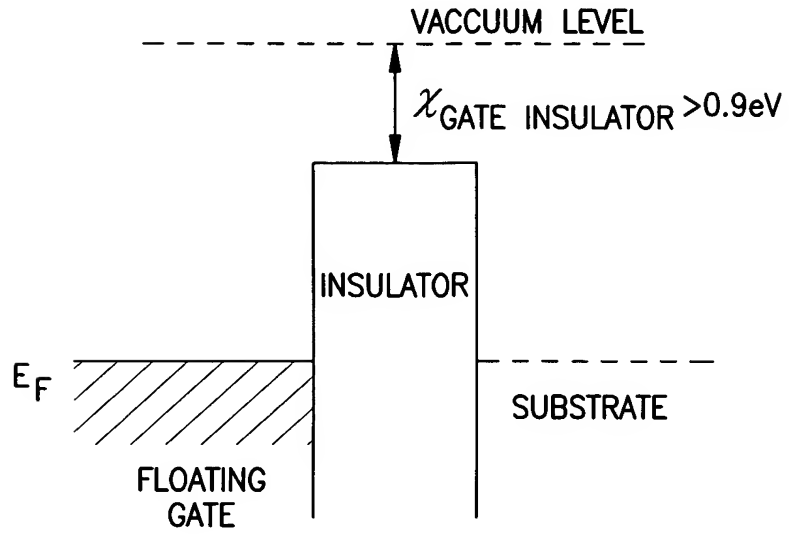

FIG. 1C
(PRIOR ART)

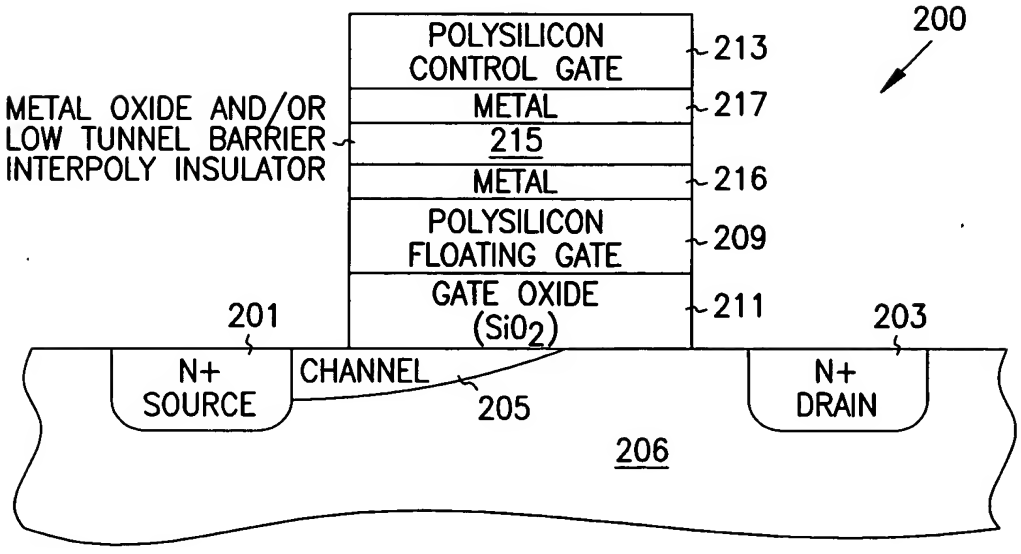

FIG. 2

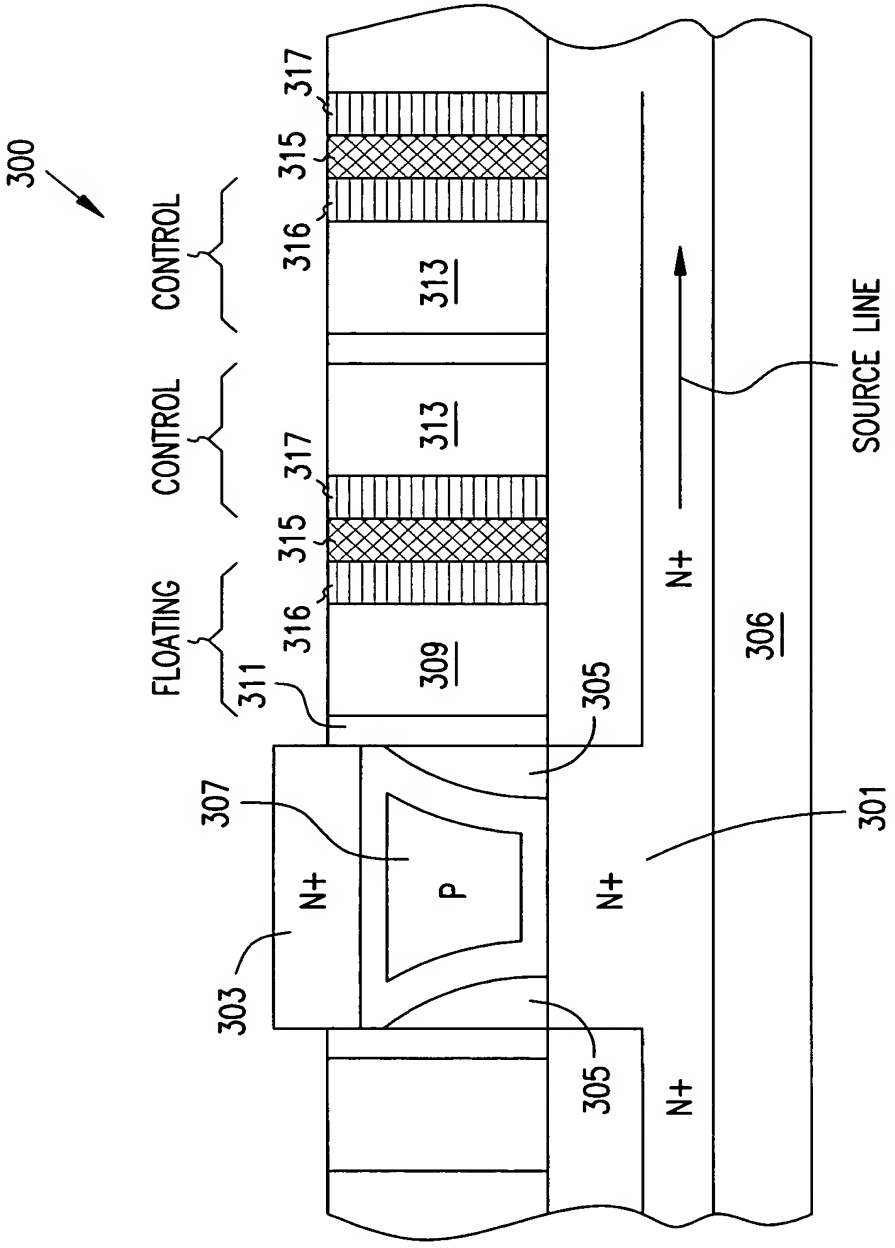
300
CONTROL
CONTROL
FLOATING
317
315
316
313
313
317
315
316
309
311
305
307
303
N+
P
N+
305
N+
306
N+
301
SOURCE LINE

FIG. 3

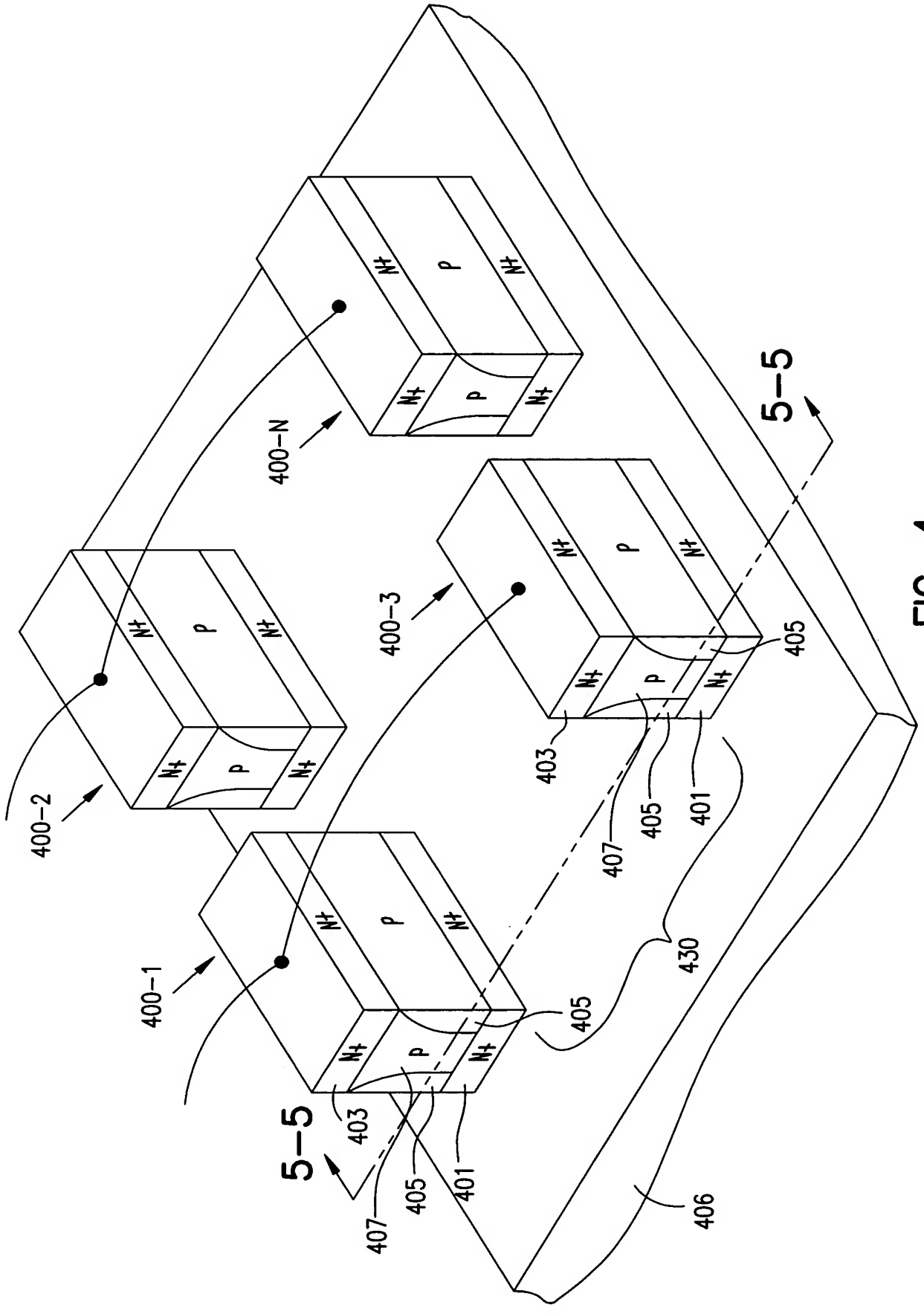

FIG. 4

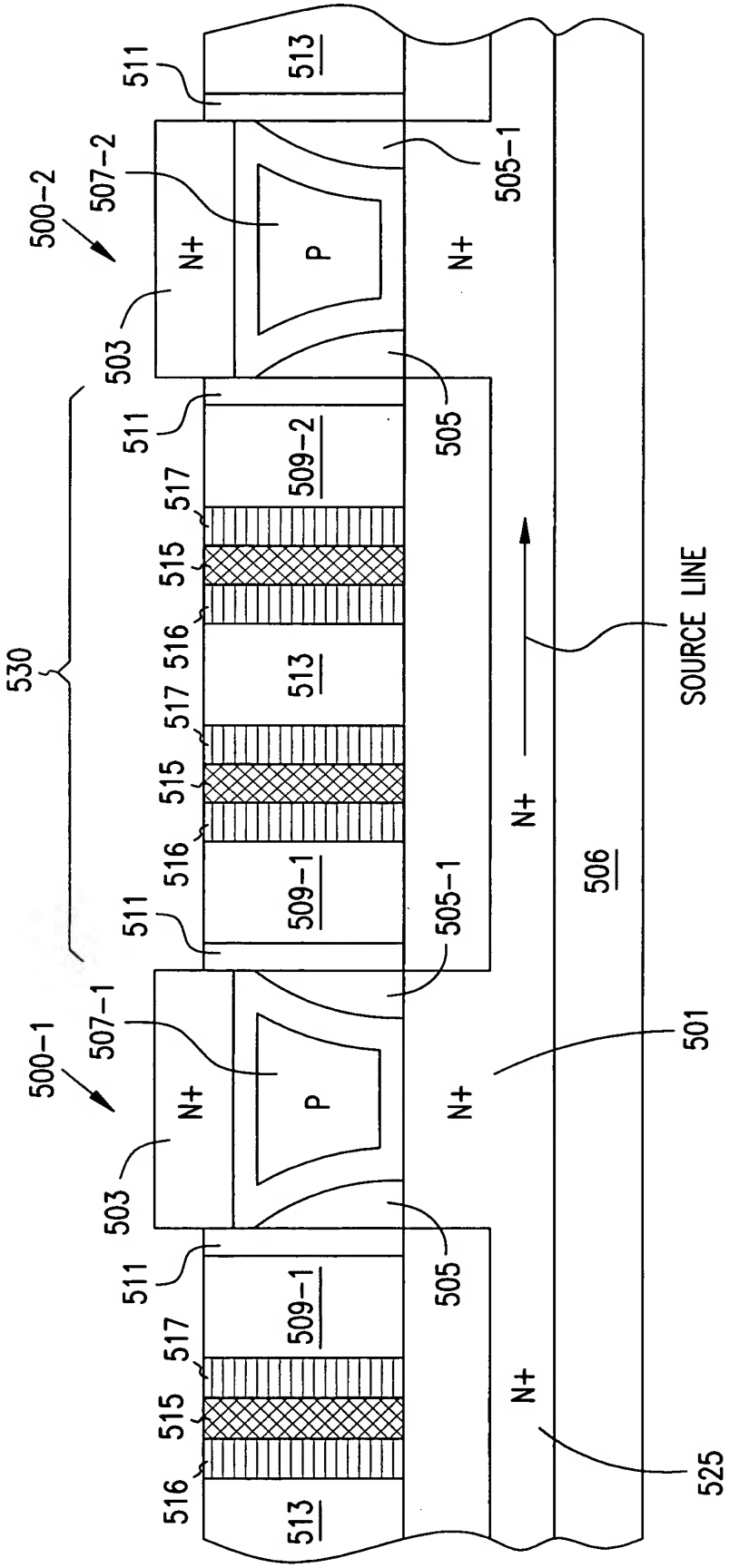
500-2
507-2
N+
P
N+
503
505-1
505
511
513
509-2
517
515
516
530
509-1
505-1
500-1
507-1
501
506
525
SOURCE LINE

FIG. 5A

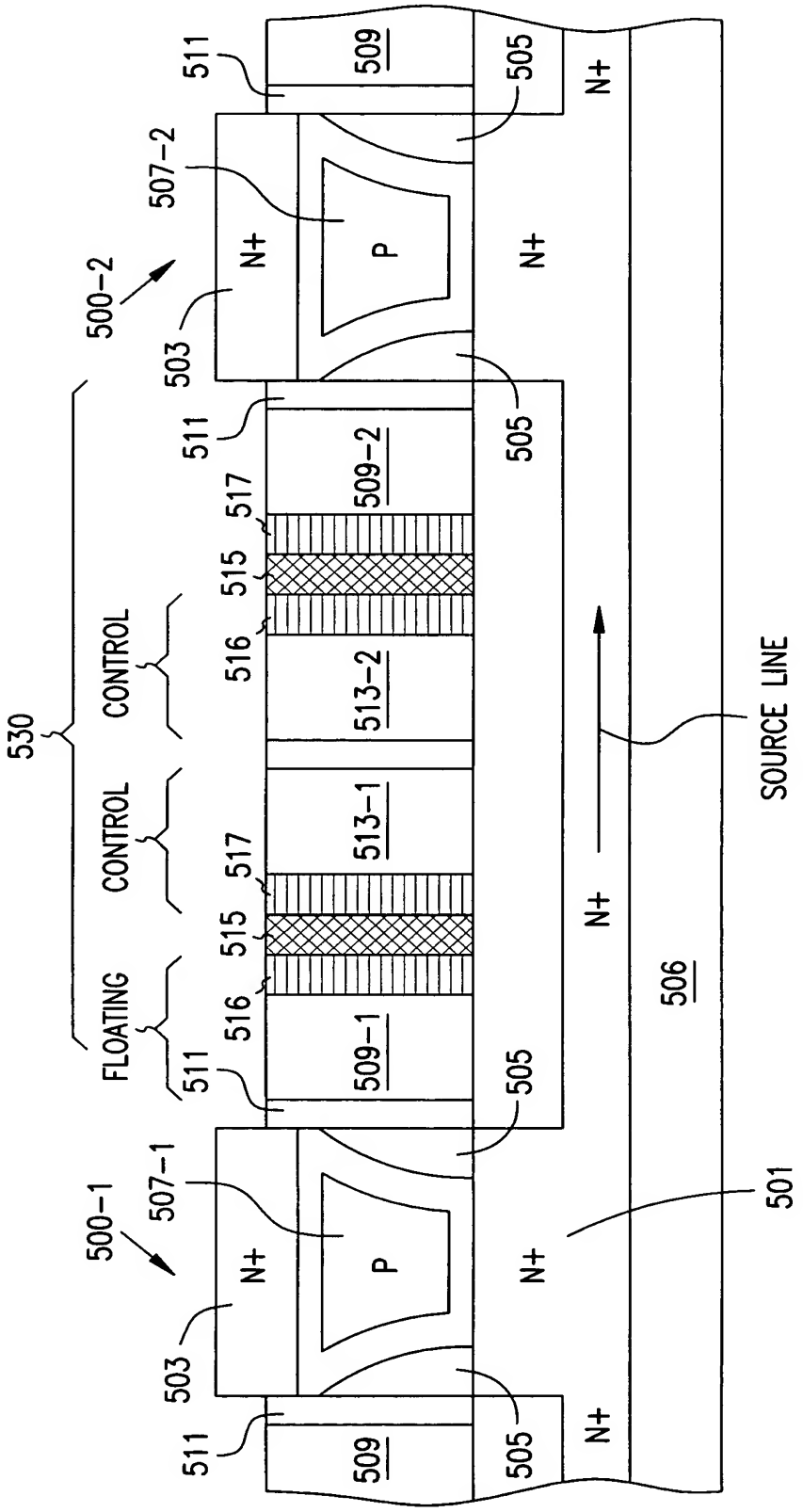
500-2
500-1
507-2
507-1
503
511
509
509-2
509-1
505
517
515
516
513-2
513-1
530
CONTROL
CONTROL
FLOATING
P
N+
506
501
SOURCE LINE

FIG. 5B

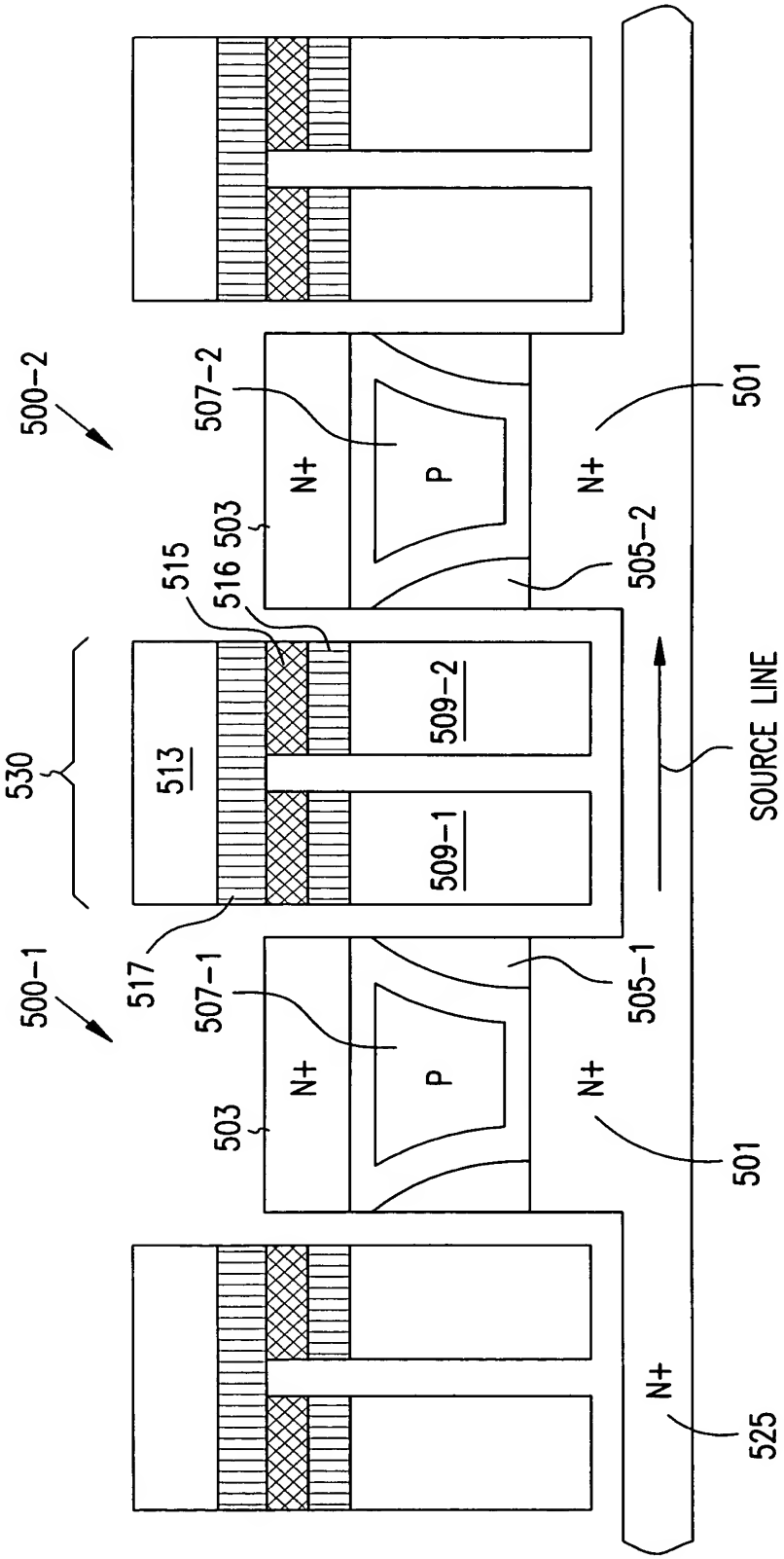
500-2
507-2
N+
P
N+
501
503
515
516
505-2
530
513
509-2
509-1
SOURCE LINE
517
500-1
507-1
505-1
503
N+
P
N+
501
N+
525

FIG. 5C

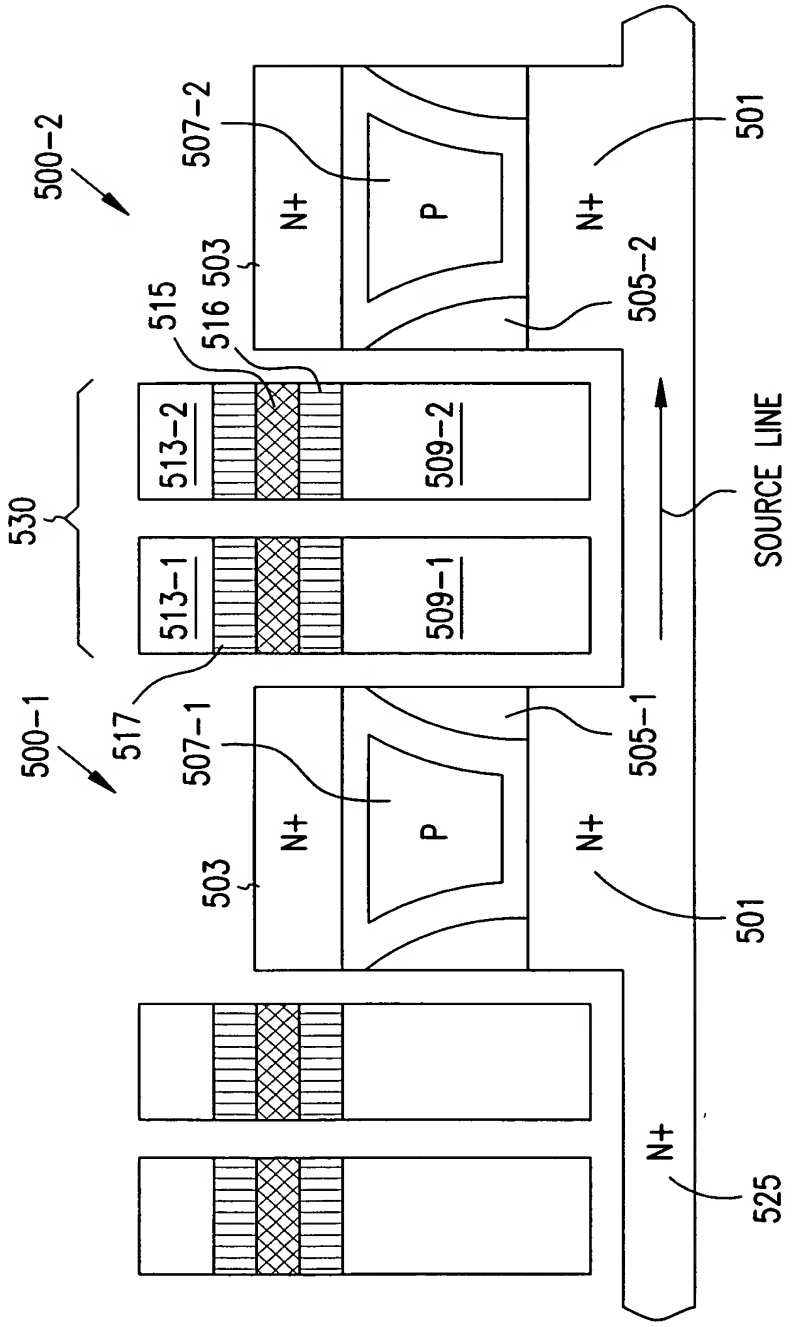
500-2
507-2
N+
P
N+
501
503
516
515
505-2
513-2
509-2
530
513-1
509-1
SOURCE LINE
500-1
517
507-1
505-1
N+
P
N+
503
501
N+
525

FIG. 5D

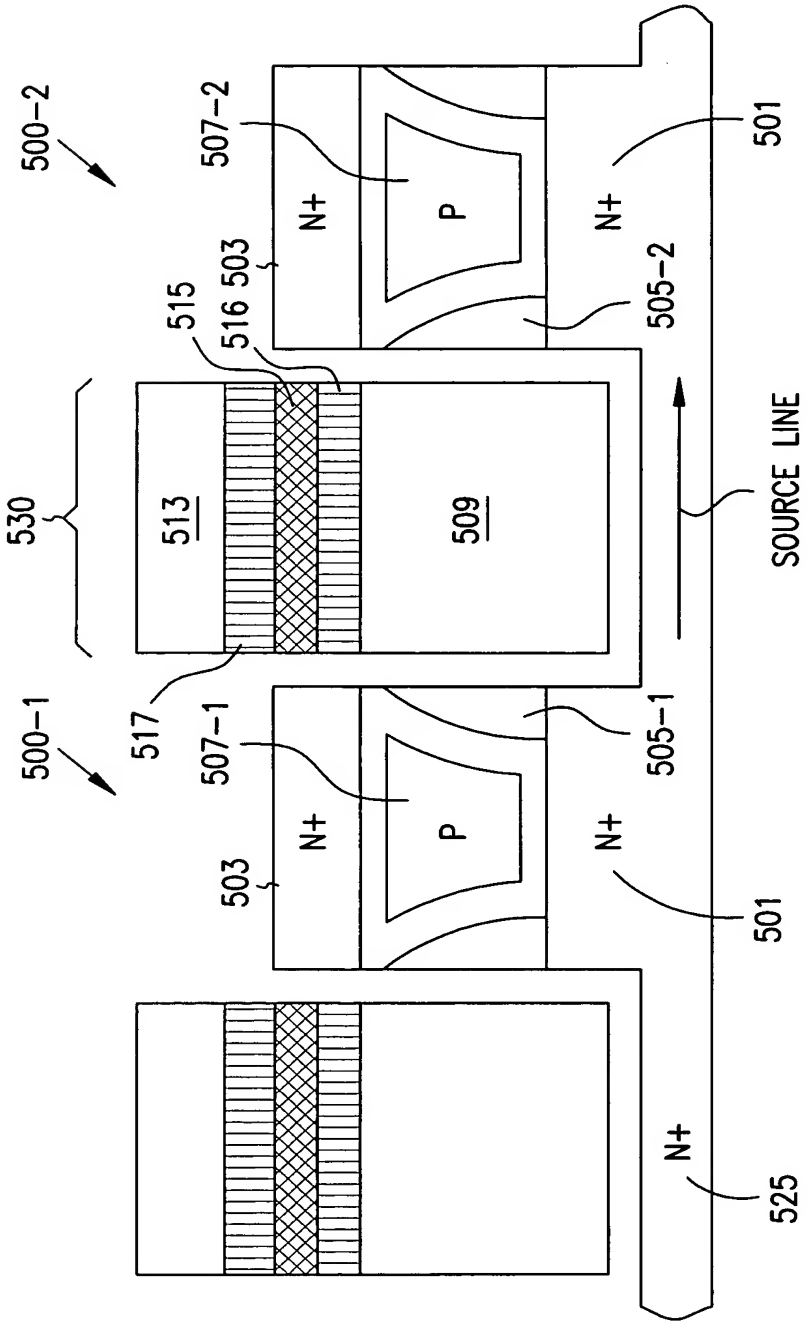
500-2
507-2
501
N+
P
N+
503
515
516
505-2
530
513
509
SOURCE LINE
517
500-1
507-1
505-1
N+
P
N+
503
501
N+
525

FIG. 5E

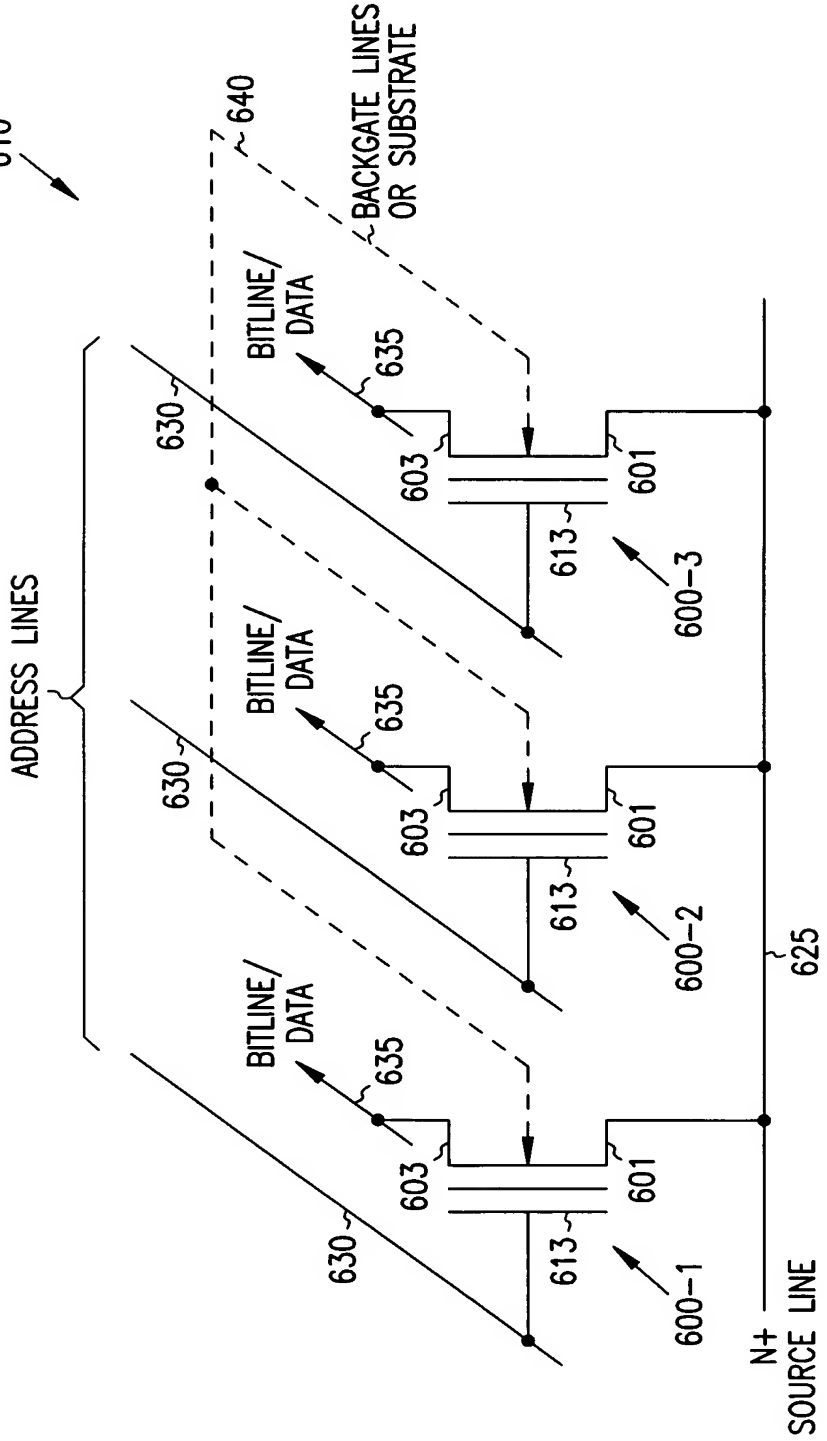
610
640
BACKGATE LINES OR SUBSTRATE
ADDRESS LINES
BITLINE/ DATA
635
630
603
601
613
600-3
600-2
600-1
625
N+ SOURCE LINE

FIG. 6A

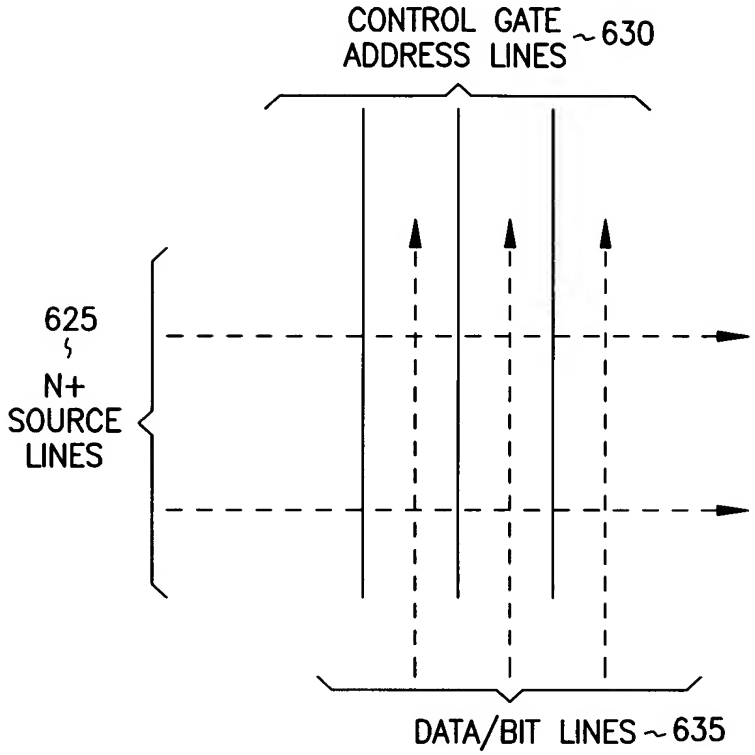
CONTROL GATE ADDRESS LINES ~630
625
N+ SOURCE LINES
DATA/BIT LINES ~635

FIG. 6B

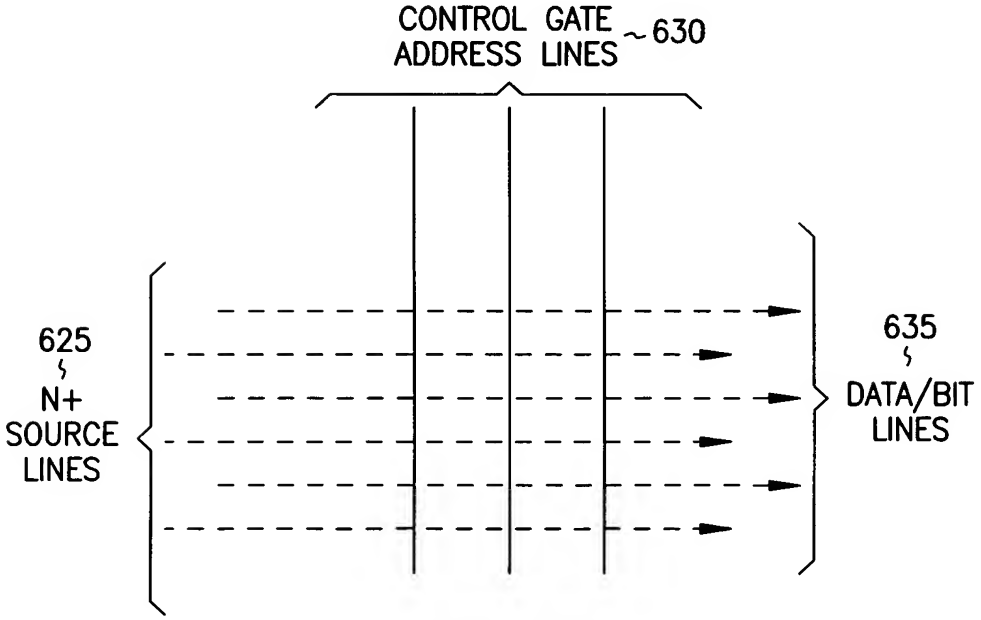
CONTROL GATE ADDRESS LINES ~630
625
N+ SOURCE LINES
635
DATA/BIT LINES

FIG. 6C

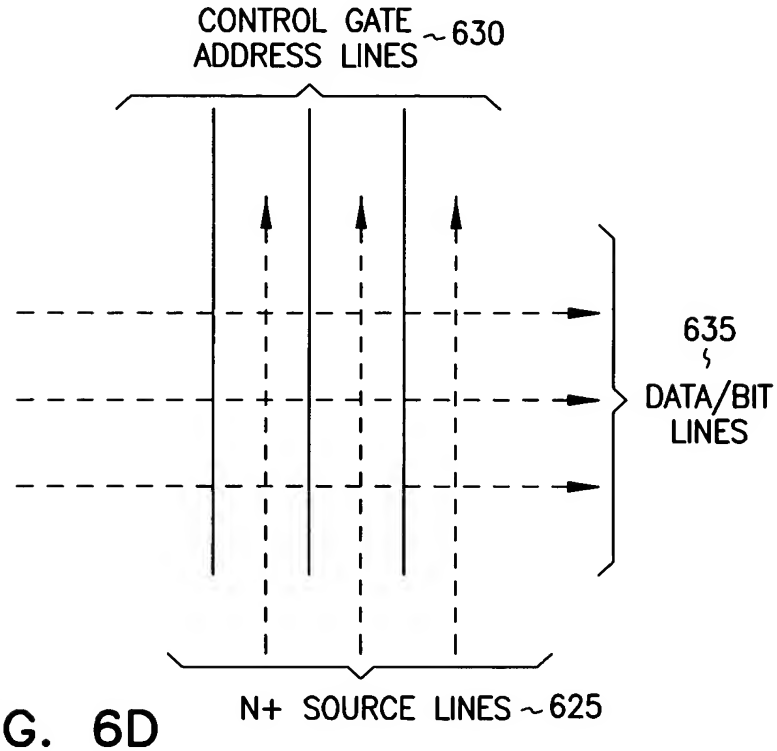
CONTROL GATE ADDRESS LINES ~630
635
DATA/BIT LINES
N+ SOURCE LINES ~625

FIG. 6D

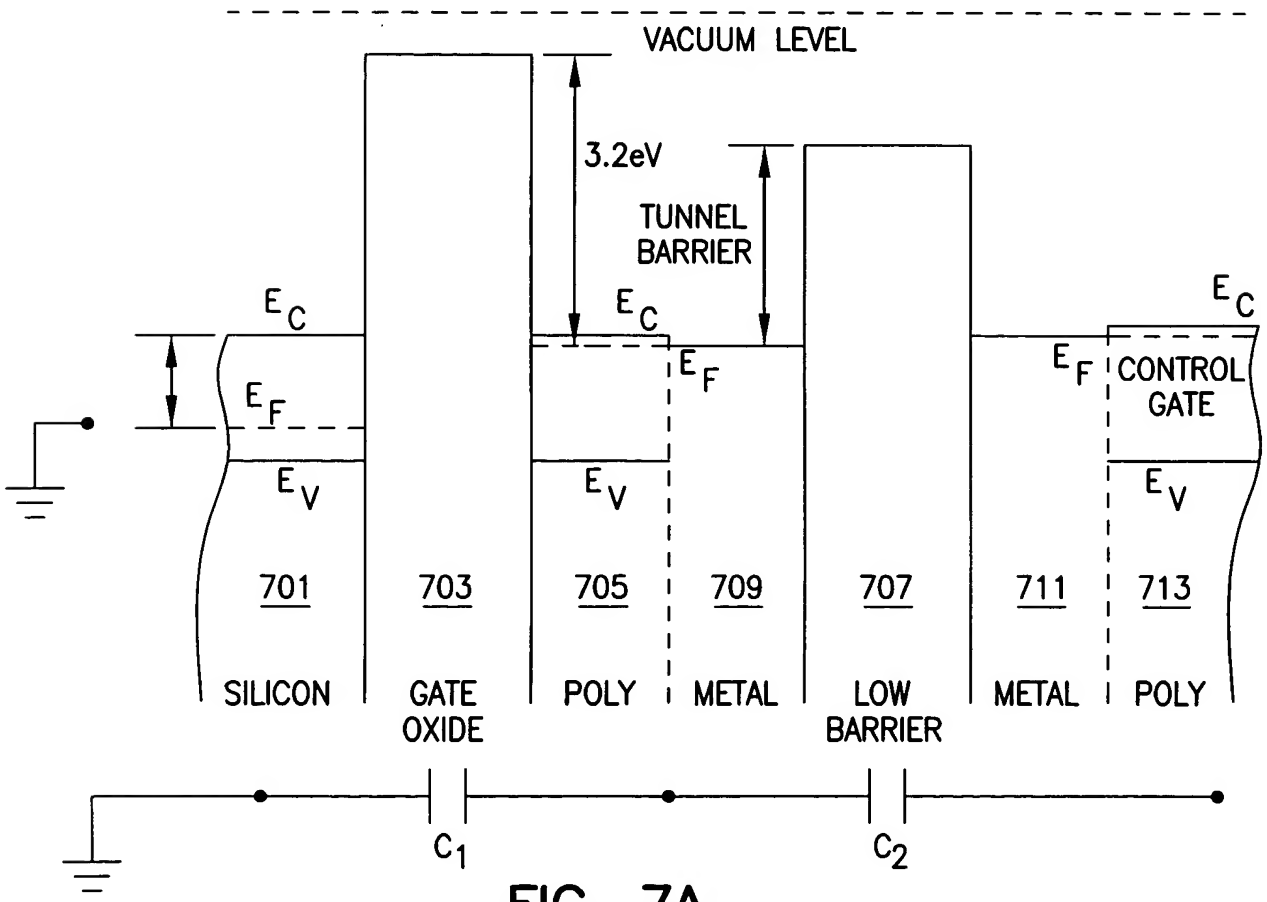
VACUUM LEVEL
3.2eV
TUNNEL BARRIER
E_C
E_F
E_V
CONTROL GATE
701
703
705
709
707
711
713
SILICON
GATE OXIDE
POLY
METAL
LOW BARRIER
METAL
POLY
C_1
C_2

FIG. 7A

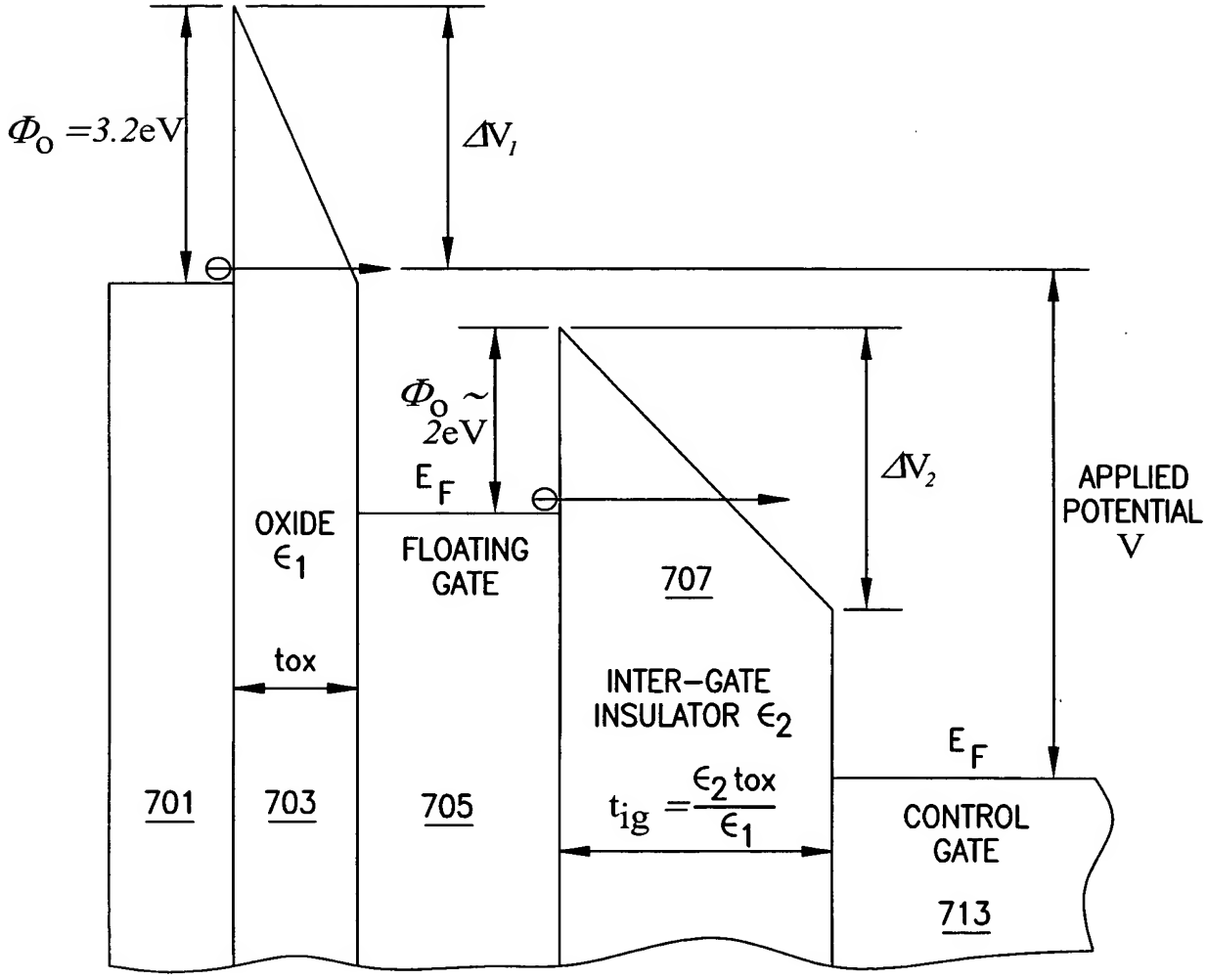
$\Phi_0 = 3.2\text{eV}$
ΔV_1
$\Phi_0 \sim 2\text{eV}$
E_F
ΔV_2
APPLIED POTENTIAL V
OXIDE ϵ_1
FLOATING GATE
707
tox
INTER-GATE INSULATOR ϵ_2
E_F
701
703
705
$t_{ig} = \frac{\epsilon_2 \text{ tox}}{\epsilon_1}$
CONTROL GATE
713

FIG. 7B

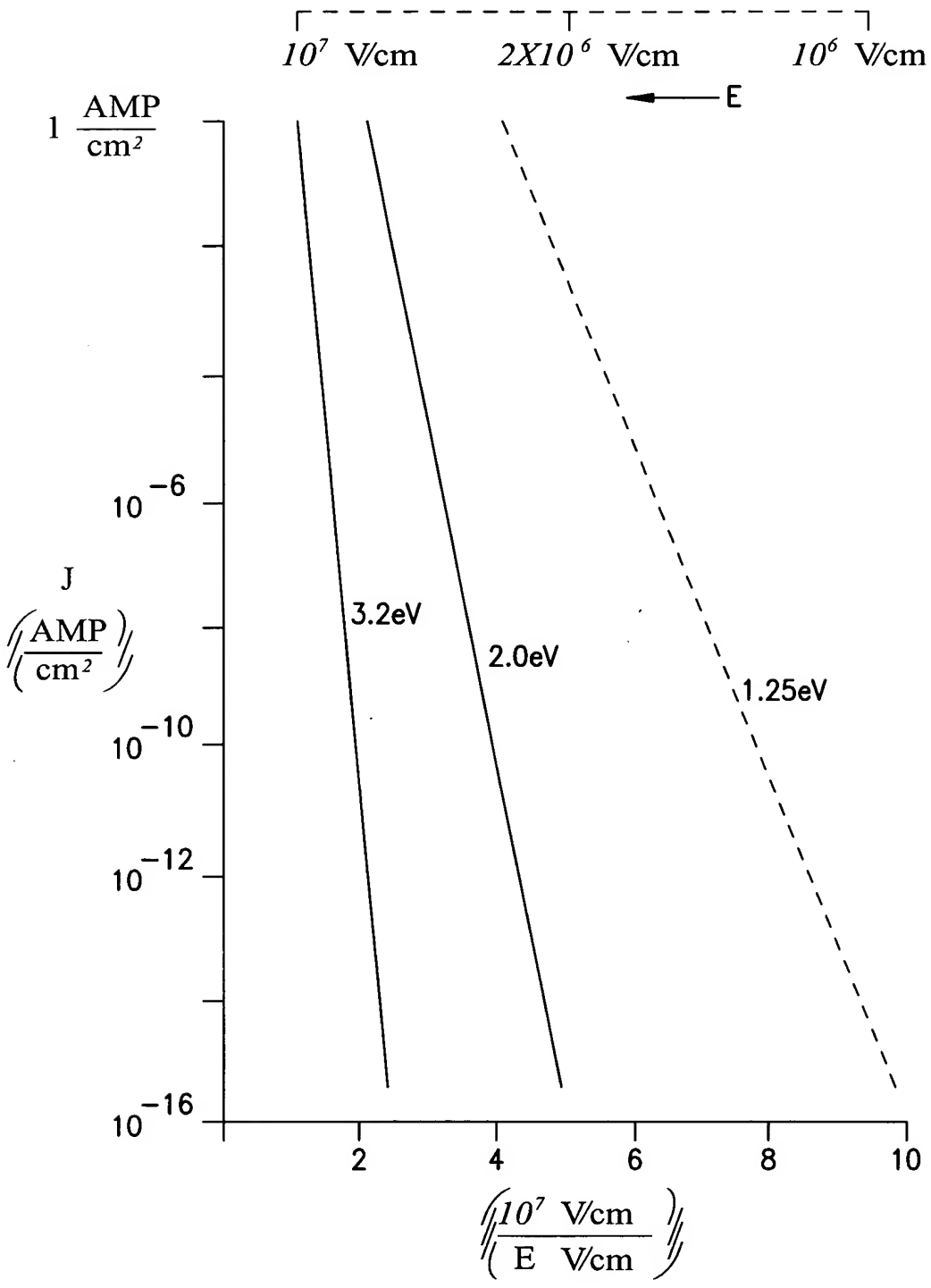
10^7 V/cm
$2X10^6$ V/cm
10^6 V/cm
E
1 AMP/cm²
10^{-6}
10^{-10}
10^{-12}
10^{-16}
J (AMP/cm²)
3.2eV
2.0eV
1.25eV
2
4
6
8
10
10^7 V/cm / E V/cm

FIG. 7C

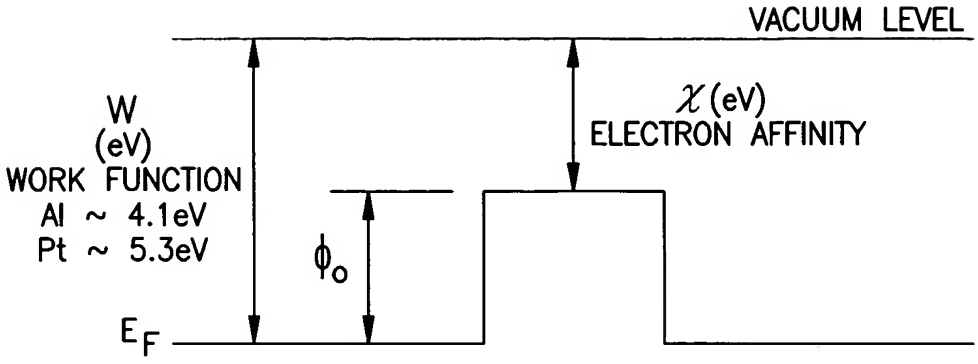
VACUUM LEVEL
W
(eV)
WORK FUNCTION
Al ~ 4.1eV
Pt ~ 5.3eV
χ (eV)
ELECTRON AFFINITY
ϕ_o
E_F

FIG. 8

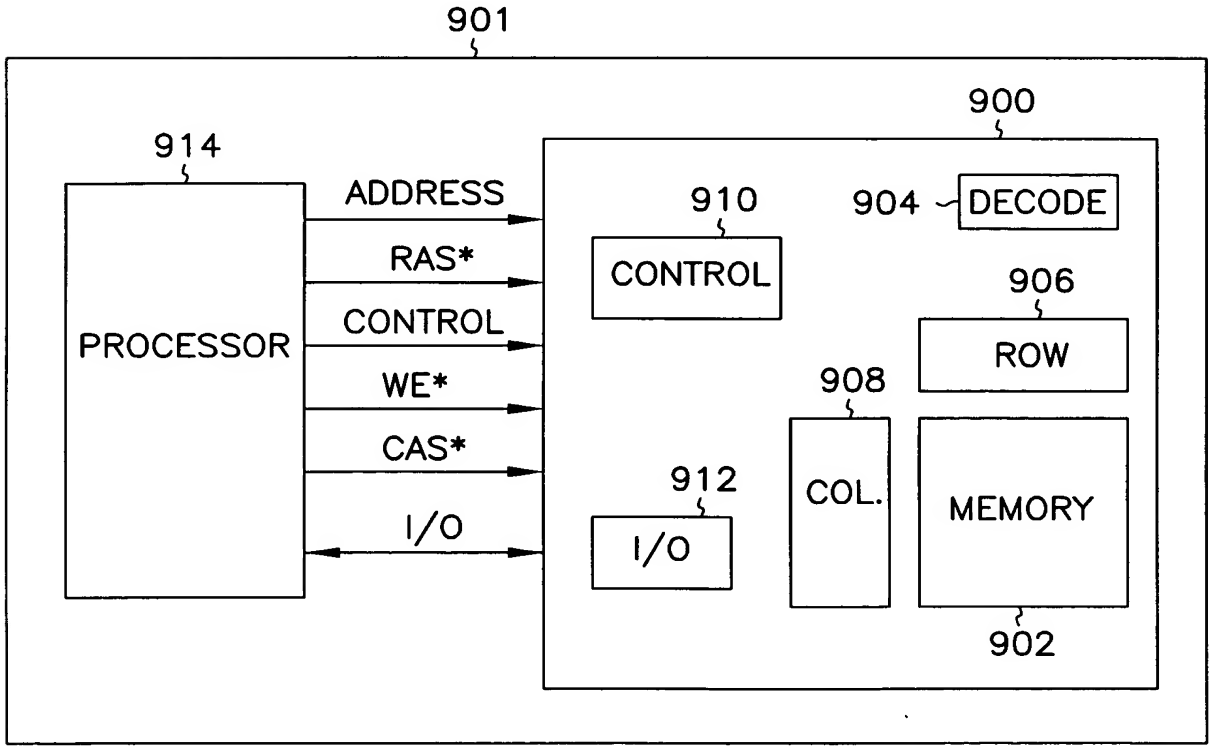
901
900
914
PROCESSOR
ADDRESS
RAS*
CONTROL
WE*
CAS*
I/O
910
CONTROL
904
DECODE
906
ROW
908
COL.
912
I/O
MEMORY
902

FIG. 9